

Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) EP 0 959 568 A1

(12)

EUROPEAN PATENT APPLICATION

published in accordance with Art. 158(3) EPC

(43) Date of publication:

24.11.1999 Bulletin 1999/47

(51) Int. Cl.⁶: H04B 3/10

(21) Application number: 97905438.4

(86) International application number:

PCT/JP97/00653

(22) Date of filing: 04.03.1997

(87) International publication number:

WO 98/39854 (11.09.1998 Gazette 1998/36)

(84) Designated Contracting States:
DE FR GB

• MURAKAMI, Keishi,
Mitsubishi Denki KK
Tokyo 100 (JP)

(71) Applicant:
MITSUBISHI DENKI KABUSHIKI KAISHA
Tokyo 100 (JP)

(74) Representative:
Pfenning, Meinig & Partner
Mozartstrasse 17
80336 München (DE)

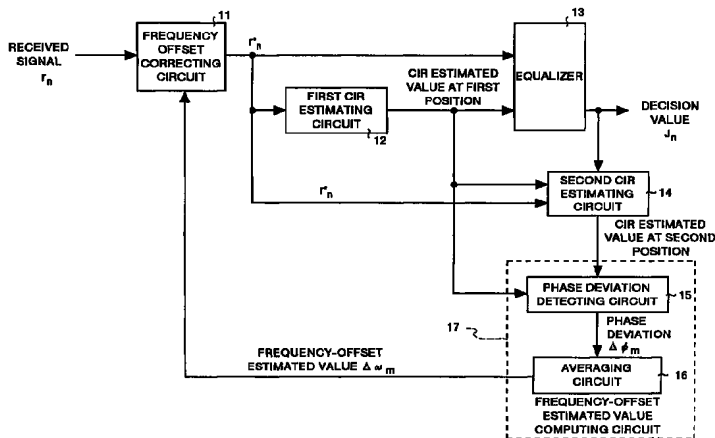
(72) Inventors:
• NAGAYASU, Takayuki,
Mitsubishi Denki KK
Tokyo 100 (JP)

(54) RECEIVER WITH FREQUENCY OFFSET CORRECTING FUNCTION

(57) Distortion of a received signal due to intersymbol interference as well as to frequency offset is corrected. For this reason, a frequency offset correcting circuit 21 corrects a received signal based on a frequency-offset estimated value. A first CIR estimating circuit 22 estimates CIR estimated values at a first position according to a known training sequence in the corrected received signal. Also, a second estimating circuit 24 updates the CIR estimated values with the LMS algorithm according to the corrected received signals as well as to the decision value outputted from the equal-

izer 13 with the CIR estimated values at the first position as initial values and obtains CIR estimated values at a second position apart from the first position. A phase deviation detecting circuit 15 computes phase deviations based on CIR estimated values at the first position as well as on CIR estimated values at the second position, and an averaging circuit 26 averages the phase deviations, and outputs the averaged value to the frequency offset correcting circuit 21 as a frequency-offset estimated value.

FIG.1



EP 0 959 568 A1

Description

TECHNICAL FIELD

5 [0001] The present invention relates to a receiver with a frequency offset correcting function used for radio digital data transfer such as that for an automobile telephone.

BACKGROUND ART

10 [0002] Prior to description of the prior art, description is made for a technological background concerning the present invention.

[0003] Fig. 14 shows a model of a channel with intersymbol interference (ISI) therein.

[0004] The model expresses a channel with a finite impulse response (FIR) filter. In the model, a received signal is a synthesized signal synthesized from a lead signal with the output thereof directly received and a delay signal with the output thereof received with a delay due to its reflection or so.

[0005] In the figure, a time difference between delay signals is given by a delay circuit DELAY comprising L-segmented shift register. The lead signal is obtained by multiplying a transmitted signal I_n by channel impulse response (CIR) $c_{0,n}$ as a tap coefficient with a multiplier MULT0. Herein, a subscript n of CIR $c_{0,n}$ indicates a time of data received during TDMA communications.

20 [0006] Also, delay signals are obtained by multiplying delayed transmitted signals I_{n-1} to I_{n-L} by tap coefficients $c_{1,n}$ to $c_{L,n}$ with multipliers MULT1 to L respectively. Then, outputs of delay signals from the multipliers MULT0 to L are summed up by a summing device SUM, and an adder (ADD) adds noise W_n to the summed wave outputted from the summing device (SUM) to output the added wave as a received signal r_n .

[0007] When intersymbol interference (ISI) is not present in the channel, the received signal r_n is expressed with the following equation.

$$r_n = c_{0,n} I_n + W_n \quad (1)$$

[0008] In this case, $c_{0,n}$ is a known value, so that a transmitted signal I_n can easily be estimated from a received signal r_n on condition that a noise W_n is small.

30 [0009] By the way, according to the model in Fig. 14, when a transmitted sequence of $\{I_n\}$ is transmitted to the channel, this transmitted sequence undergoes intersymbol interference (ISI) in addition to additive white Gaussian noise W_n in the channel. Accordingly, the received signal r_n includes not only a time n but also a transmitting sequence I_n in the past before that time. The received signal at this time is expressed with the following equation:

$$r_n = \sum c_{i,n} I_{n-i} + W_n \quad (2)$$

wherein the sum \sum is obtained for values of $i = 0, \dots, L$, and L indicates a time length affected by intersymbol interference (ISI), namely a channel memory length.

40 [0010] In the model of the channel shown in Fig. 14, the transmitted sequence I_n includes a range from time n to time (n-L). An equalizer is often used for the channel described above as a device for estimating a transmitted sequence I_n from a received signal r_n .

[0011] Also, when there is frequency offset $\Delta \omega$ generated due to a difference between a local oscillator of a transmitter and a local oscillator of a receiver, a received signal is expressed with the following equation:

$$r_n = \sum c_{i,n} I_{n-i} \exp(\Delta \omega n + \theta_0) + W'_n \quad (3)$$

wherein θ_0 is an initial phase, and W'_n is expressed with the following equation:

$$W'_n = W_n \exp(\Delta \omega n + \theta_0) \quad (4)$$

[0012] As described above, the performance of a receiver is deteriorated due to distortion caused by frequency offset $\Delta \omega$ in addition to intersymbol interference (ISI). And for this reason, the receiver needs to correct the intersymbol interference (ISI) and also the distortion caused by frequency offset $\Delta \omega$.

55 [0013] Next description is made for an example of a receiver with a frequency offset correcting function based on the conventional technology.

[0014] Fig. 15 is a block diagram showing the conventional type of receiver for correcting frequency offset. The receiver in this example is the same as that described in "Method and Device for Compensating Carrier Frequency Off-

set in TDMA Communication System (Japanese Patent Laid-open Publication No. HEI 6-508244)" disclosed by Lin Yuphan et al.

[0015] In Fig. 15, designated at the reference numeral 211 is a CIR estimating circuit for estimating CIR according to a training sequence in a received signal, at 212 a phase deviation detecting circuit for computing a phase deviation according to the CIR estimated value estimated by the CIR estimating circuit 211 and a tail bit described later of the received signal, at 213 an averaging circuit for averaging the phase deviations outputted from the phase deviation detecting circuit 212 and computing a frequency offset estimated value, at 214 a frequency offset correcting circuit for correcting the received signal r_n according to the frequency offset estimated value outputted from the averaging circuit 213, and at 215 an equalizer for equalizing a data sequence in the received signal according to the received signal r'_n corrected by the frequency offset correcting circuit 214 as well as to the CIR estimated value outputted from the CIR estimating circuit 211, and determining, when a binary signal, for instance, 1 or -1 is transmitted, which value of 1 and -1 is the received signal r_n or the like.

[0016] Fig. 16 shows a burst B1 of received signals received during TDMA communications based on the conventional technology shown in Fig. 15.

[0017] In the figure, this burst B1 comprises a training sequence B11, data sequence B12, B13, and tail bits B14, B15, and the training sequence B11 and the tail bits B14, B15 are known in the receiver side.

[0018] Next description is made for operations in the example based on the conventional technology with reference to Fig. 15 and Fig. 16.

[0019] At first, the CIR estimating circuit 211 computes, when having received a received signal r_n , CIR estimated values g_0, g_1, \dots, g_L according to the training sequence B11 in the received burst B1 as shown in Fig. 16 as well as to the training sequence having previously been known in the receiver side.

[0020] Then, the phase deviation detecting circuit 212 first computes a phase deviation ϕ_m with the following equation according to the CIR estimated values g_0, g_1, \dots, g_L estimated with the known training sequence in the received burst B1 by the CIR estimating circuit 211 as well as to the known tail bits $I_{n-L}, I_{n-L+1}, \dots, I_n$. It should be noted that a subscript m in the equation indicates a phase deviation in the burst of a m -th received signal.

$$s_n = \sum g_i I_{n-i} \quad (5)$$

$$\phi_m = \{ \text{Im}[r_n] \cdot \text{Re}[s_n] - \text{Im}[s_n] \cdot \text{Re}[r_n] \} / \{ \text{ABS}[r_n] \cdot \text{ABS}[s_n] \} \quad (6)$$

wherein the sum Σ is obtained for $i = 0, \dots, L$. It should be noted that L indicates, as shown in the channel model in Fig. 14, a time length affected by intersymbol interference (ISI), namely a channel memory length, and corresponds to the number of stages in the delay circuit DELAY. Also, in the equation, designated at the reference sign s_n is a replica (estimated value) of a received signal, at $\text{Re}[a]$ a real part of a complex number a , at $\text{Im}[a]$ an imaginary part of the complex number a , and at $\text{ABS}[a]$ an absolute value of the complex number a respectively.

[0021] Further, the phase deviation detecting circuit 212 computes a phase deviation per symbol $\Delta \phi_m$ through the following equation according to the phase deviation ϕ_m as described above, and outputs a result of the computing to the averaging circuit 213.

$$\Delta \phi_m = \phi_m \{ 2 / (M - 1) \} \quad (7)$$

wherein M indicates a total number of symbols of a received burst B1.

[0022] Then, the averaging circuit 213 averages the phase deviation per symbol $\Delta \phi_m$ estimated for each burst B1, and outputs a result of averaging to the frequency offset correcting circuit 214 as a frequency-offset estimated value ω_m .

[0023] The frequency offset correcting circuit 214 corrects frequency offset of a received signal r_n through the following equation according to the frequency-offset estimated value $\Delta \omega_m$.

$$r'_n = r_n \exp (-j \Delta \omega_m n) \quad (8)$$

[0024] The equalizer 215 determines data according to the received signal r'_n having been subjected to offset correction outputted from the frequency offset correcting circuit 214 as well as to the CIR estimated value outputted from the CIR estimating circuit 211, and outputs a result of the decision as a decision value.

[0025] However, in the receiver with the conventional type of frequency offset correcting function, known data such as tail bits other than the training sequence is required to compute a frequency-offset estimated value, and also a length of tail bits in a received signal is generally required to be longer than a memory length L of the channel, so that transmission efficiency is worse in turn by the length required for the tail bits.

[0026] In the example based on the conventional technology, a phase deviation is computed according to the CIR

estimated value, the tail bits in the received signal and the estimated value (replica) of the bits, so that the phase deviation to be detected largely varies with noises. Accordingly, in order to estimate frequency offset with sufficient precision, it is required to suppress variation by making a time constant larger for averaging phase deviations, and for this reason, when frequency offset varies with time, it is difficult to follow the variation in the method described above.

5 [0027] Further, as diversity reception is not performed in the example based on the conventional technology, an error rate in decision is higher as compared to the case where diversity reception is performed.

[0028] The present invention has been made for solving the problems as described above, and it is an object of the present invention to provide a receiver with a frequency offset correcting function which has improved the capabilities of being excellent in transmission efficiency without requiring known data other than a training sequence, precisely estimating time-varying frequency offset, and further enabling performance of diversity reception and determination of data at a low error rate.

DISCLOSURE OF INVENTION

15 [0029] To achieve the object as described above, the present invention comprises a frequency offset correcting means for receiving a received signal as well as a frequency-offset estimated value and correcting phase rotation due to frequency offset of the received signal according to the frequency-offset estimated value; a first channel impulse response estimating means for estimating channel impulse response at a first position of the corrected received signal according to a known training sequence included in the received signal corrected by the frequency offset correcting means; a determining means for determining the received signal corrected by the frequency offset correcting means according to the channel impulse response estimated value at the first position thereof estimated by the first channel impulse response estimating means; a second channel impulse response estimating means for estimating channel impulse response at a second position apart from the first position of the corrected received signal according to the received signal corrected by the frequency offset correcting means, the channel impulse response estimated value at the first position thereof estimated by the first channel impulse response estimating means, and to the value determined by the determining means; and a frequency-offset estimated value computing means for computing a frequency-offset estimated value of the received signal according to the channel impulse response estimated value at the first position thereof estimated by the first channel impulse response estimating means as well as to the channel impulse response estimated value at the second position thereof estimated by the second channel impulse response estimating means, and outputting the computed value to the frequency offset correcting circuit. Therefore, with this invention, different channel-impulse estimated values at the first and second positions are obtained according to the training sequence having been known in the received signal, and a frequency-offset estimated value is computed according to those phase deviations, so that frequency offset of a received signal can be corrected and also data can be determined without using known data such as tail bits other than the training sequence. As a result, tail bits are not needed as a burst structure of a received signal, so that transmission efficiency is improved, and also a phase deviation can be computed not according to an estimated value (replica) of the received signal computed only with tail bits in a transmission sequence but according to channel impulse response estimated by sufficiently suppressing a noise element with an appropriate algorithm (e.g., LMS algorithm), and for this reason a phase deviation to be detected does not largely varies with noises, time-varying frequency offset can be compensated with high precision, and data can be determined at a low error rate.

[0030] The another present invention comprises a frequency offset correcting means for receiving a received signal as well as a frequency-offset estimated value and correcting phase rotation due to frequency offset of the received signal according to the frequency-offset estimated value; a first channel impulse response estimating means for estimating channel impulse response at a first position of the corrected received signal according to a known training sequence included in the received signal corrected by the frequency offset correcting means; a determining means for determining the received signal corrected by the frequency offset correcting means; a second channel impulse response estimating means for estimating channel impulse response at a second position apart from the first position of the corrected received signal by updating the channel impulse response estimated value at the first position according to the received signal corrected by the frequency offset correcting means, the channel impulse response estimated value at the first position thereof estimated by the first channel impulse response estimating means, and to the value determined by the determining means; and a frequency-offset estimated value computing means for computing a frequency-offset estimated value of the received signal according to the channel impulse response estimated value at the first position thereof estimated by the first channel impulse response estimating means as well as to the channel impulse response estimated value at the second position thereof estimated by the second channel impulse response estimating means, and outputting the computed value to the frequency offset correcting circuit; and the determining means determines the received signal corrected by the frequency offset correcting means, at first, according to the channel impulse response estimated value at the first position thereof estimated by the first channel impulse response estimating means, and determines the received signal corrected by the frequency offset correcting means, after the second time

and on, according to a value updated from the channel impulse response estimated value at the first position thereof by the second channel impulse response estimating means. For this reason, with this invention, determination of the received signal after the second time and on is made according to values obtained, by successively updating the channel impulse response estimated value at the first position, outputted from the second estimating means, so that, even when the channel impulse response estimated value varies with time, the variation can be followed, and data can be determined at a low error rate.

[0031] The another present invention comprises a first channel impulse response estimating means for estimating channel impulse response at a first position of the received signal according to a known training sequence included in the received signal; a determining means for determining the received signal corrected by the frequency offset correcting means according to the channel impulse response estimated value at the first position thereof estimated by the first channel impulse response estimating means; a second channel impulse response estimating means for estimating channel impulse response at a second position apart from the first position of the received signal according to the received signal corrected by the frequency offset correcting means, the channel impulse response estimated value at the first position thereof estimated by the first channel impulse response estimating means, and to the value determined by the determining means; a frequency-offset estimated value computing means for computing a frequency-offset estimated value of the received signal according to the channel impulse response estimated value at the first position thereof estimated by the first channel impulse response estimating means as well as to the channel impulse response estimated value at the second position thereof estimated by the second channel impulse response estimating means; and a local oscillator correcting means for correcting a frequency from a local oscillator according to the frequency-offset estimated value computed by the frequency-offset estimated value computing means. Therefore, with this invention, a frequency from the local oscillator of the receiver is directly controlled in place of correcting frequency offset of the received signal, so that configuration of the circuit can be simplified.

[0032] The another present invention comprises a frequency offset correcting means for receiving a plurality of received signals as well as frequency-offset estimated value, and correcting each phase rotation due to frequency offset for the plurality of received signals according to the frequency-offset estimated value respectively; a first channel impulse response estimating means for estimating each channel impulse response at a first position of the plurality of corrected received signals according to each known training sequence included in the plurality of received signals corrected by the frequency offset correcting means; a determining means for determining the plurality of received signals corrected by the frequency offset correcting means according to the channel impulse response estimated values each at the first position thereof estimated by the first channel impulse response estimating means; a second channel impulse response estimating means for estimating each channel impulse response at a second position apart from the first position of the plurality of corrected received signals according to the plurality of received signals corrected by the frequency offset correcting means, each channel impulse response estimated value at the first position of the plurality of corrected received signals estimated by the first channel impulse response estimating means, and to the value of the plurality of received signals determined by the determining means; and a frequency-offset estimated value computing means for computing frequency-offset estimated value of the plurality of received signals according to each channel impulse response estimated value at the first position thereof estimated by the first channel impulse response estimating means as well as to each channel impulse response estimated value at the second position thereof estimated by the second channel impulse response estimating means, and outputting the computed value to the frequency offset correcting circuit. Therefore, with this invention, a plurality of received signals can be received with a plurality of frequency offset correcting circuits or the like respectively, so that diversity reception can be performed, and data can be determined at a low error rate.

[0033] In the present inventions, the frequency-offset estimated value computing means comprises a phase deviation detecting means for detecting a phase deviation between the first position and the second position according to the channel impulse response estimated value at the first position estimated by the first channel impulse response estimating means as well as to the channel impulse response estimated value at the second position estimated by the second channel impulse response estimating means; and an averaging means for averaging phase deviations obtained by computing a phase deviation per symbol according to the phase deviation between the first position and the second position detected by the phase deviation detecting means to compute a frequency-offset estimated value, and outputting the computed value to the frequency offset correcting circuit.

[0034] Also, the phase deviation detecting means selects a value of which the absolute value is the maximum among the channel impulse response estimated values at the first position estimated by the first channel impulse response estimating means, and also selects a value corresponding to the channel impulse response estimated value at the first position of which the absolute value is the maximum among the channel impulse response estimated values at the second position estimated by the second channel impulse response estimating means; and detects a phase deviation of the received signal according to the product of complex conjugate of the channel impulse response estimated value at the first position of which the absolute value is the maximum and the channel impulse response estimated value at the second position corresponding to the channel impulse response estimated value at the first position of which the abso-

lute value is the maximum.

[0035] Also, the phase deviation detecting means computes each product of the complex conjugate of the channel impulse response estimated value at the first position estimated by the first channel impulse response estimating means and the channel impulse response estimated value at the second position estimated by the second channel impulse response estimating means, and detects a phase deviation of the received signal according to the sum of the products each of which the absolute value is more than a threshold value among the computed products.

[0036] Also, the phase deviation detecting means computes each product of the complex conjugate of the channel impulse response estimated value at the first position estimated by the first channel impulse response estimating means and the channel impulse response estimated value at the second position estimated by the second channel impulse response estimating means, selects each product of which the absolute value is more than a threshold value among the computed products, multiplies each of the absolute values to the selected products, and detects the phase deviation of the received signals according to the sum of the multiplied values.

[0037] Also, the phase deviation detecting means further quantizes the phase deviation of the detected received signal, and outputs a result of the quantization as a phase deviation.

[0038] Also, the determining means comprises a soft-decision equalizer for executing soft-decision of a data sequence in the corrected received signal according to the received signal corrected by the frequency offset correcting means as well as to the channel impulse response estimated value at the first position estimated by the first channel impulse response estimating means; and a hard-decision circuit for executing hard decision of the soft-decision value estimated by the soft-decision equalizer and outputting a result of the decision as a decision value of a data sequence in the received signal. Therefore, with this invention, decision can be made including reliability by the soft-decision equalizer, so that the reliability can be utilized in forward error correction and so on.

BRIEF DESCRIPTION OF DRAWINGS

[0039] Fig. 1 is a block diagram showing configuration of a receiver with a frequency offset correcting function according to Embodiment 1 of the present invention; Fig. 2 is a view showing a burst structure of the received signal in Embodiment 1; Fig. 3 is a view showing configuration of a determining circuit 13a having an equalizer for executing soft-determination in place of equalizer 13; Fig. 4 is a view showing another method of computing a CIR estimated value at the second position; Fig. 5 is a view showing another method of computing a CIR estimated value at the second position; Fig. 6 is a view showing another method of computing a CIR estimated value at the second position; Fig. 7 is a view showing another method of computing a CIR estimated value at the second position; Fig. 8 is a view showing another method of computing a CIR estimated value at the second position; Fig. 9 is a view showing another method of computing a CIR estimated value at the second position; Fig. 10 is a view showing a graph of a quantizing function; Fig. 11 is a block diagram showing configuration of a receiver with a frequency offset correcting function according to Embodiment 2 of the present invention; Fig. 12 is a block diagram showing configuration of a receiver with a frequency offset correcting function according to Embodiment 3 of the present invention; Fig. 13 is a block diagram showing configuration of a receiver with a frequency offset correcting function according to Embodiment 4 of the present invention; Fig. 14 is a block diagram showing a model of a channel with intersymbol interference (ISI) therein; Fig. 15 is a block diagram showing configuration of the receiver with a frequency offset correcting function based on the conventional technology; and Fig. 16 is a view showing a burst structure of a received signal in the example based on the conventional technology.

BEST MODE FOR CARRYING OUT THE INVENTION

(1) Embodiment 1

[0040] At first, description is made for a receiver with a frequency offset correcting function according to Embodiment 1 of the present invention.

[0041] Fig. 1 is a block diagram showing configuration of the receiver with the frequency offset correcting function according to Embodiment 1 of the present invention.

[0042] In the figure, designated at the reference numeral 11 is a frequency offset correcting circuit for correcting a received signal r_n with a frequency-offset estimated value $\Delta \omega_m$ outputted from an averaging circuit 16 described later; at 12 a first CIR estimating circuit for estimating CIR at a first position on a burst according to a training sequence in a received signal r'_n corrected by the frequency offset correcting circuit 11; at 13 an equalizer as a determining means for equalizing a data sequence in the received signal according to the received signal r'_n corrected by the frequency offset correcting circuit 11 as well as to the CIR estimated value at the first position estimated by the first CIR estimating circuit 12, and determining, when a binary signal of, for instance, 1 or -1 is received, which value of 1 and -1 is the received signal r_n or the like; at 14 a second CIR estimating circuit for estimating a CIR estimated value at a second position

apart from the first position on the burst in a corrected received signal r'_n according to the received signal r'_n corrected by the frequency offset correcting circuit 11, the CIR estimated value at the first position estimated by the first CIR estimating circuit 12, and to a result of decision by the equalizer 13; at 15 a phase deviation detecting circuit for computing a phase deviation according to the CIR estimated value at the first position estimated by the first CIR estimating circuit 12 as well as to the CIR estimated value at the second position estimated by the second CIR estimating circuit 14; and at 16 an averaging circuit for averaging the phase deviations detected by the phase deviation detecting circuit 15 and computing a frequency offset estimated value. It should be noted that the phase deviation detecting circuit 15 and averaging circuit 16 constitute a frequency-offset estimated value computing circuit 17.

[0043] Fig. 2 shows a burst B2 of the received signal r_n in

Embodiment 1.

[0044] In the figure, the burst B2 of the received signal r_n in Embodiment 1 comprises a training sequence B21 known in the receiver and data sequence B22, and does not include tail bits different from the burst B1 having been described in the conventional technology shown in Fig. 16.

[0045] In the figure, designated at the reference sign n is a time, at P1 a time M1, namely a first position indicating a symbol of the time corresponding to a final symbol of the training sequence B21 in the burst B2, at P2 a second position indicating a symbol of a time M2, and M0 is a time indicating a length of all the symbols in this burst B2.

[0046] It should be noted that the burst B2 may also include tail bits similarly to the case of the burst B1 based on the conventional technology, but the present invention has eliminated the need for tail bits because frequency offset of a received signal is computed and corrected only based on the training sequence without using the tail bits.

[0047] Next description is made for operations of the receiver with a frequency offset correcting function configured as described above according to Embodiment 1. Further, it is assumed that the burst B2 is received as received signal shown in Fig. 2.

[0048] At first, the frequency offset correcting circuit 11 corrects a received signal r_n at a time $m-1$ one time interval before the time m as described later based on the frequency-offset estimated value $\Delta \omega_{m-1}$ having been estimated by the averaging circuit 16 through the following equation.

$$r'_n = r_n \exp (-j \Delta \omega_{m-1} n) \quad (9)$$

[0049] Then, the first CIR estimating circuit 12 computes CIR estimated values $g_{0,n}, g_{1,n}, \dots, g_{L,n}$ with an LMS (Least Mean Square) algorithm according to the known training sequence l_n as well as to the training sequence B21 in the corrected received signal r'_n . It should be noted that the LMS algorithm is as follows:

$$g_{i,n} = g_{i,n-1} + \alpha \{r'_n - \sum g_{j,n-1} l_{n-j}\} l_{n-i}^* \quad (10)$$

wherein i and n indicate as follows: $i = 0, \dots, L$, and $n = L+1, \dots, M1$. Also, the sum Σ is obtained for $j = 0, \dots, L$, and the reference sign a^* indicates a complex conjugate of a complex number a . The reference sign α indicates a step size of the LMS algorithm, and initial values $g_{0,L}, g_{1,L}, \dots, g_{L,L}$ of the CIR estimated values are set to arbitrary values respectively.

[0050] It should be noted that the reference sign L indicates, as described in the conventional technology, a time length affected by intersymbol interference (ISI) in the transmission model in Fig. 14, namely a channel memory length. The reference sign $M1$ indicates a time corresponding to the final symbol of the training sequence in the burst B2 and is a first position where the first CIR is estimated.

[0051] Then, the equalizer 13 determines a data sequence according to the CIR estimated values $g_{0,M1}, g_{1,M1}, \dots, g_{L,M1}$ outputted from the first CIR estimating circuit 12 as well as to the corrected received signal r'_n , and outputs a result of the decision as a decision value J_n . It should be noted that the decision value J_n indicates not a decision value outputted at the time n but a decision value corresponding to the transmitted signal l_n . Namely, J_n will be equal to l_n on condition that appropriate decision is made.

[0052] Then, the second CIR estimating circuit 14 updates the CIR estimated values $g_{0,n}, g_{1,n}, \dots, g_{L,n}$ with the LMS algorithm according to the corrected received signal r'_n as well as to the decision value J_n outputted from the equalizer 13 with the CIR estimated values $g_{0,M1}, g_{1,M1}, \dots, g_{L,M1}$, as initial values, at the first position P1 in the burst B2 outputted from the first CIR estimating circuit 12, namely at the time M1 corresponding to the final symbol of the training sequence B21 in the burst B2 as shown in Fig. 2; estimates CIR estimating values $g_{0,M2}, g_{1,M2}, \dots, g_{L,M2}$ at the second position P2 which is apart from the first position, namely at the time M2 apart from the time M1 corresponding to the final symbol of the training sequence B21 in the burst B2 as shown in Fig. 2; and outputs the estimated values to the phase deviation detecting circuit 15. It should be noted that the CIR estimated values $g_{0,n}, g_{1,n}, \dots, g_{L,n}$ with the LMS algorithm are updated with the following equation:

$$g_{i, n} = g_{i, n-1} + \alpha \{r_n^* - \sum g_{j, n-1} J_{n-j}\} J_{n-i}^* \quad (11)$$

wherein i and n indicate as follows: $i = 0, \dots, L$, and $n = M1 + 1, \dots, M2$. Also, the sum Σ is obtained for $j = 0, \dots, L$. As for J_n in $n \leq M1$, the training sequence I_n is used in place of the decision value J_n .

[0053] The phase deviation detecting circuit 15 detects, when having received a CIR estimated value at the second position P2 from the second CIR estimating circuit 14, a phase deviation according to the sequence described below.

[0054] Namely, at first, any CIR estimated value of which the absolute value is maximum is selected as a tap coefficient among the CIR estimated values $g_{0, M1}, g_{1, M1}, \dots, g_{L, M1}$ at the first position on the burst B2 outputted from the first CIR estimating circuit 12. Herein, it is assumed that a CIR estimated value of which the absolute value is maximum is a tap coefficient $g_{Max, M1}$.

[0055] Also, the CIR estimated value $g_{i, M2}$ corresponding to the tap coefficient $g_{Max, M1}$, namely i of which is the same as that of $g_{Max, M1}$, is selected as a tap coefficient $g_{Max, M2}$ among the CIR estimated values $g_{0, M2}, g_{1, M2}, \dots, g_{L, M2}$ at the second position apart from the first position on the burst B2 outputted from the second estimating circuit 14, and a phase deviation Φ_m on a complex plane is computed with the following equation:

$$\Phi_m = g_{Max, M2} \cdot g_{Max, M1}^* \quad (12)$$

[0056] Then, the phase deviation Φ_m on the complex plane is converted to a phase deviation ϕ_m on polar coordinates with the following equation:

$$\phi_m = \text{Im}[\Phi_m] / \text{Re}[\Phi_m] \quad (13)$$

[0057] Then, the averaging circuit 16 divides the phase deviation ϕ_m outputted from the phase deviation detecting circuit 15 by $(M2 - M1)$ to compute the phase deviation $\Delta \phi_m$ per symbol.

$$\Delta \phi_m = \phi_m / (M2 - M1) \quad (14)$$

[0058] Further, the averaging circuit 16 averages the phase deviation $\Delta \phi_m$ per symbol obtained as described above with a FIR filter expressing with the following equation, and outputs a result of the averaging as a frequency-offset estimated value $\Delta \omega_m$ to the frequency offset correcting circuit 11:

$$\Delta \omega_m = \Sigma \Delta \phi_{m-j} / Q \quad (15)$$

wherein the sum Σ is obtained for $j = 1, \dots, Q$. It should be noted that Q is the number of samples of $\Delta \phi_{m-j}$ when the values $\Delta \phi_{m-j}$ are averaged with the FIR filter. That is because each of the values $\Delta \phi_{m-j}$ is displaced from the actual value due to fading and noises, so that the values $\Delta \phi_{m-j}$ estimated at different times are averaged to reduce the displacement from the actual value. For this reason, the larger the value of Q is, the smaller the variation of $\Delta \omega_m$ is, and for this reason, a stable value can be obtained, but actually, when an amount of frequency offset varies with time, response to the variation may be delayed, performance of tracking the variation to a degree of fluctuation of $\Delta \omega_m$ can be affected depending on the value of Q , so that, in this case, the value of Q should not be so large.

[0059] Then, the frequency offset correcting circuit 11 corrects a received signal r_n to be inputted according to a frequency-offset estimated value $\Delta \omega_m$ from the averaging circuit 16 through the equation (9).

[0060] As described above, with Embodiment 1 of the present invention, frequency offset is estimated without using known data such as tail bits other than the training sequence, and data can be determined while distortion of the frequency offset is compensated, so that the need for the known data such as tail bits other than the training sequence can be eliminated, transmission efficiency can be improved, and there is no need for suppressing variation by making a time constant larger for averaging a phase deviation to estimate frequency offset with sufficient precision, and for this reason, even when frequency offset varies with time, the variation can easily be followed, and time-varying frequency offset can be estimated with high precision.

[0061] Also, in Embodiment 1, a phase deviation is detected based on a CIR estimated value at the first position P1 estimated according to the known training sequence and a training sequence in a received signal as well as on a CIR estimated value at the second position P2 apart from the first position obtained by updating this CIR estimated value at the first position with the LMS algorithm, so that, by making a step size of the LMS algorithm smaller, CIR estimated values at both of the first position and the second position in which noise elements included in the received signal are sufficiently suppressed can be obtained, and frequency offset can be corrected with frequency-offset estimated values having less noise element.

[0062] As a result, in Embodiment 1, a phase deviation can precisely be detected, which allows a time constant for averaging to be made smaller and time-varying frequency offset to be estimated with high precision.

[0063] It should be noted that detailed description is not made for operations of the equalizer 13 in Embodiment 1 of the present invention because the invention is not in relation to the equalizer 13 itself as a determining means, but there is one example of the operations of an equalizer as described in detail with maximum-likelihood sequence estimation (MLSE) disclosed in "Maximum-likelihood sequence estimation of digital sequence in presence of intersymbol interference" by G. D. Forney, Jr. (IEEE trans. Information Theory, vol. IT-18, pp. 363-378, May 1972).

[0064] As the equalizer 13, a non-linear equalizer and a linear equalizer such as a decision-feedback equalizer may be used.

[0065] Also, in addition to the LMS algorithm, a RLS (Recursive Least Squares) algorithm and modified algorithms of the LMS algorithm and the RLS algorithm may be used for updating of the CIR estimated values by the second estimating circuit 14.

[0066] Also, in Embodiment 1, although the phase deviation $\Delta \phi_m$ per symbol is computed in the averaging circuit 16, a computing method can also be changed so that the phase deviation $\Delta \phi_m$ per symbol is computed in the phase deviation detecting circuit 15 like in the conventional technology. The computing method can also be changed so that a frequency-offset estimated value $\Delta \omega_m$ is computed by averaging a phase deviation ϕ_m in the averaging circuit 16 and dividing a result of the averaging by $(M2-M1)$.

[0067] Also, in Embodiment 1, in place of the equalizer 13 as a decision means, as shown in Fig. 3, a decision circuit 13a comprising a combination of a soft-decision equalizer 13a1 for outputting soft-decision value with a hard-decision circuit 13a2 for hard-decision a soft-decision value described in "Optimum and sub-optimum detection of coded data distributed by time-varying intersymbol interference (IEEE GLOBECOM' 90, San Diego, pp. 1679-1685, Dec. 1990) by W. Koch et al. or the like may be provided.

[0068] Herein, although detailed description is not made for the soft-decision equalizer because the present invention is not made for the soft-decision equalizer itself, the equalizer 13 in Embodiment 1 determines which of 1 and -1 is transmitted from a received signal, what is called, makes hard decision, while the soft-decision equalizer 13a1 determines received signals by assigning weights to received signals including reliability of the received signals, namely depending on the reliability of the received signals, and a result of the decision is outputted at multivalues such as 1.2, 0.3, and -0.5. Then, the hard-decision circuit 13a2 makes hard-decision, namely determines which of 1 and -1 the transmitted signal is in the case described above according to the decision output from the soft-decision equalizer 13a1 and outputs a decision value J_n .

[0069] Also, in Embodiment 1, the second CIR estimating circuit 14 updates a CIR estimated value at the first position which is the time $M1$ estimated by the first CIR estimating circuit 12 according to the decision value J_n obtained from $n = M1 + 1 \sim M2$ in the burst $B1$ of the received signal shown in Fig. 2, estimates a CIR estimated value at the second position apart from the first position, namely the time $M2$, and a phase deviation of the received signal is computed from the two CIR estimated values, but in the present invention, a phase deviation may be computed by estimating CIR estimated values at the first and second positions with the methods shown in Fig. 4 to Fig. 9 described later.

[0070] Specifically, as shown in Fig. 4, the first position where the first CIR estimating circuit 12 estimates a CIR estimated value is the time $M1$ of the final symbol of the training sequence $B21$, which is not changed, but the second CIR estimating circuit 14 may compute a phase deviation according to the first CIR estimated value and the second CIR estimated value by updating a CIR estimated value according to a decision value J_n obtained from $n = M3 + 1 \sim M0$ with CIR estimated values $g_{0, M1}, g_{1, M1}, \dots, g_{L, M1}$ at the first position $P1$ at the time $M1$ estimated by the first CIR estimating circuit 12 as initial values, regarding the time $M0$, namely the final symbol position of the data sequence $B22$ in the burst $B2$ as the second position $P2$, and estimating a CIR estimated value at the second position $P2$ thereof.

[0071] As shown in Fig. 5, in a case of the burst $B3$ with its structure comprising a training sequence $B31$ and data sequence 32 and 33, a CIR estimated value at the second arbitrary position $P2$ in the data sequence $B32$ may be computed through the same processing as that in Embodiment 1 by obtaining a CIR estimated value at a first arbitrary position in the data sequence $B33$ by means of the same processing as that in Embodiment 1 according to the CIR estimated value at the time of the final symbol in the training sequence $B31$ and reversing the series on its time axis according to the CIR estimated value at the time of a header symbol in the training sequence $B31$.

[0072] It should be noted that, in this case of the burst $B3$, a phase deviation may also be computed by using only the training sequence $B31$ and data sequence $B33$ with the CIR estimated value at the first position which is a time corresponding to the final symbol of the training sequence $B31$ as well as with the CIR estimated value at the second arbitrary position of the training sequence $B31$ by means of the same processing as that in Embodiment 1 shown in Fig. 2.

[0073] As shown in Fig. 6, in a case of the burst $B3$ comprising the training sequence $B31$ and the data sequence 32 and 33 which are the same as those shown in Fig. 5, for the training sequence $B31$ and the data sequence 33, a position of the final symbol in the data sequence $B33$ is regarded as the first position $P1$ and a CIR estimated value may be computed at the position through the same processing as that in Fig. 3, and also for the training sequence $B31$ and data sequence $B32$, a position of the header symbol in the data sequence $B32$ is also regarded as the second position $P2$ and a CIR estimated value may be computed through the same processing as that in Fig. 3 by reversing the sequence on its time axis.

[0074] It should be noted that, in this case of the burst B3, a phase deviation may also be computed by using only the training sequence B31 and data sequence B33 through the same processing as the method described in Embodiment 1 shown in Fig. 2 and the method shown in Fig. 4.

[0075] As shown in Fig. 7, in a case of the burst B2 comprising the training sequence B21 and the data sequence B22, CIR estimated values at a plurality of the second positions such as positions P21 to P24 are computed based on the CIR estimated value at the first position P1 through the same processing as that in Embodiment 1, each phase deviation is obtained with the CIR estimated values at adjacent positions to each other, and the average value of those phase deviations may be outputted to the averaging circuit 16 as a result of the phase deviations. In this case, even when the burst B2 comprising the training sequence B21 and the data sequence B22 shown in Fig. 7 is used, a plurality of phase deviations are obtained, the plurality of phase deviations are averaged, and the averaged value is outputted to the averaging circuit 16 as a phase deviation, so that a more accurate phase deviation of a received signal can be obtained.

[0076] As shown in Fig. 8, in a case of the burst B3 comprising the training sequence B31 and the data sequence B32 and B33, CIR estimated values, for instance, at the plurality of positions P21 to P24 in the data sequence B33 are obtained and CIR estimated values, for instance, at the plurality of positions P21' to P24' in the data sequence B31 are obtained by regarding the header or the tail of the training sequence B32 as each of the first positions P1 and P1' and based on the CIR estimated values at the positions, a plurality of phase deviations are obtained from the CIR estimated values at the adjacent position to each other, the plurality of phase deviations are averaged, and the averaged value may be outputted to the averaging circuit 16 as a phase deviation. In this case, even when the burst B3 comprising the training sequence B31 and the data sequence B32 and B33 is used, similarly to the case shown in Fig. 7, a plurality of phase deviations are obtained, the plurality of phase deviations are averaged, and the averaged value is outputted to the averaging circuit 16 as a phase deviation, so that a more accurate phase deviation of a received signal can be obtained.

[0077] In a case of a burst B4 in which data sequence as shown in Fig. 9 are continued, a CIR estimated value at the position P1 of the known training sequence B41 is obtained similarly to the case in Embodiment 1 shown in Fig. 2, CIR estimated values at a plurality of positions such as positions P2 to P5 are computed based on the CIR estimated value at the first position P1, a plurality of phase deviations are obtained from the CIR estimated values at adjacent positions to each other, the plurality of phase deviations are averaged, and the average value may be outputted to the averaging circuit 16 as a phase deviation. In this case, even when the burst B4 with the data sequence continued as shown in Fig. 9 is used, similarly to the case in the Embodiment 7, a plurality of phase deviations are obtained, the plurality of phase deviations are averaged, and the averaged value is outputted to the averaging circuit 16 as a phase deviation, so that a more accurate phase deviation of a received signal can be obtained.

[0078] Also, the phase deviation detecting circuit 15 may detect a phase deviation according to the method as described below.

[0079] Specifically, at first, with regard to a combination of CIR estimated values $g_{0, M1}, g_{1, M1}, \dots, g_{L, M1}$ outputted from the first CIR estimating circuit 12 with CIR estimated values $g_{0, M2}, g_{1, M2}, \dots, g_{L, M2}$ outputted from the second CIR estimating circuit 14, phase deviation $\Phi_{i, m}$ on a complex plane is computed with the following equation:

$$\Phi_{i, m} = g_{i, M2} \cdot g_{i, M1}^* \quad (16)$$

wherein i indicates as follows: $i = 0, \dots, L$.

[0080] Then, phase deviations each in which $ABS[\Phi_{i, m}]$ as absolute values of the phase deviation $\Phi_{i, m}$ is more than a certain threshold value are selected, and the sum thereof is a phase deviation $\Phi_{SUM, m}$ on the complex plane:

$$\Phi_{SUM, m} = \Sigma \Phi_{i, m} \quad (17)$$

wherein, the sum Σ of the equation (17) is obtained, as described above, for phase deviations $\Phi_{i, m}$ each of which $ABS[\Phi_{i, m}]$ is more than the threshold value. Then, a phase deviation $\Phi_{SUM, m}$ on the complex plane is converted to a phase deviation ϕ_m on polar coordinates with the following equation:

$$\phi_m = \text{Im}[\Phi_{SUM, m}] / \text{Re}[\Phi_{SUM, m}] \quad (18)$$

[0081] The phase deviation detecting circuit 15 according to Embodiment 1 may detect a phase deviation according to the method as described below.

[0082] Specifically, at first, with regard to a combination of CIR estimated values $g_{0, M1}, g_{1, M1}, \dots, g_{L, M1}$ outputted from the first CIR estimating circuit 12 with CIR estimated values $g_{0, M2}, g_{1, M2}, \dots, g_{L, M2}$ outputted from the second CIR estimating circuit 14, phase deviation $\Phi_{i, m}$ on a complex plane is computed with the following equation:

$$\Phi_{i,m} = g_{i,M2} \cdot g_{i,M1}^* \quad (19)$$

wherein i indicates as follows: $i = 0, \dots, L$.

[0083] Then, phase deviations $\Phi_{i,m}$ each in which $ABS[\Phi_{i,m}]$ as absolute values of the phase deviation $\Phi_{i,m}$ is more than a specified threshold value are selected, and the sum by assigning weights to the phase deviations with the absolute values $ABS[\Phi_{i,m}]$ is a phase deviation $\Phi_{COM,m}$ on the complex plane as shown in the following equation. With those operations, weights are assigned to the phase deviations $\Phi_{i,m}$ with the absolute values $ABS[\Phi_{i,m}]$ thereof, so that a more accurate phase deviation can be obtained.

$$\Phi_{COM,m} = \sum ABS[\Phi_{i,m}] \cdot \Phi_{i,m} \quad (20)$$

wherein the sum \sum of the equation (20) is obtained, as described above, for phase deviations each of which $ABS[\Phi_{i,m}]$ is more than the threshold value. Then, a phase deviation $\Phi_{COM,m}$ on the complex plane is converted to a phase deviation ϕ_m on polar coordinates with the following equation:

$$\phi_m = \text{Im}[\Phi_{COM,m}] / \text{Re}[\Phi_{COM,m}] \quad (21)$$

[0084] It should be noted that the equations (13), (18), and (21) executed by the phase deviation detecting circuit 15 can also be computed more accurately by being substituted in the following equation:

$$\phi_m = \arctan (\text{Im}[\Phi_m] / \text{Re}[\Phi_m]) \quad (22)$$

[0085] Further, the phase deviation detecting circuit 15 quantizes a phase deviation Φ_m with a function in which a quantized phase deviation q_m is changed step by step according to changes for each specified rate of the phase deviation Φ_m as shown in Fig. 10, and may also output a result of quantization to the averaging circuit 16 in place of the phase deviation Φ_m as a quantized phase deviation q_m .

[0086] Also, an IIR filter, a random walk filter or an N-Before-M filter other than the FIR filter can be used for averaging in the averaging circuit 16.

[0087] Further, the averaging circuit 16 outputs control data for correction of frequency offset in place of outputting a frequency-offset estimated value, and can correct the frequency offset of the received signal in the frequency offset correcting circuit 11 based on the control data.

[0088] In the first CIR estimating circuit 12, in addition to the LMS algorithm, the RLS algorithm and modified algorithms of the LMS algorithm and the RLS algorithm may be used. Further, a CIR estimated value can be computed based on a correlation between a training sequence and a training sequence in the received signal. However, when computing is carried out by using the correlation, the CIR estimated value computed with the training sequence is a value at the center of the training sequence.

[0089] The configuration of Embodiment 1 may be realized with firmware such as DSP, hardware software.

[0090] Also, the change in design as described above is also applicable to those in Embodiments 2 to 4 described below in addition to Embodiment 1.

(2) Embodiment 2

[0091] Next description is made for a receiver with a frequency offset correcting function according to Embodiment 2 of the present invention.

[0092] Fig. 11 shows configuration of the receiver with a frequency offset correcting function according to Embodiment 2. It should be noted that, in the figure, the same reference numerals are assigned to the components corresponding to those in Embodiment 1 shown in Fig. 1.

[0093] Namely, Embodiment 2 is characterized in that an equalizer 13b is provided for determining a received signal r'_n of which the frequency offset has been corrected according to a CIR estimated value at the first position from the first CIR estimating circuit 12 as well as to an updated value of the CIR estimated value at the first position outputted from the second CIR estimating circuit 14b in place of the equalizer 13 according to Embodiment 1 for determining a received signal r'_n of which the frequency offset has been corrected from the frequency offset correcting circuit according to a CIR estimated value at the first position from the first CIR estimating circuit 12. For this reason, the second CIR estimating circuit 14b is so configured as to successively update, when a CIR estimated value at the second position is to be estimated, a CIR estimated value at the first position as shown in the equation (11) based on the time n and successively output the updated values to a equalizer 13b.

[0094] Next description is made for operations of this equalizer 13b, in which this equalizer 13b does not receive an updated value of a CIR estimated value only for the first time from a second CIR estimating circuit 14b, so that the

equalizer 13b equalizes a received signal r'_n corrected by the frequency offset correcting circuit 11 according to the CIR estimated values $g_{i, M1}$ outputted from the first CIR estimating circuit 12, and determines a data sequence in the received signal.

[0095] Then, as updated values of the CIR estimated values $g_{i, n}$ ($n = M1 + 1, \dots, M2$) are successively sent from the second CIR estimating circuit 14b at the second timing and thereafter, the equalizer 13 determines a received signal r'_n corrected by the frequency offset correcting circuit 11 according to the CIR estimated values $g_{i, n}$ ($n = M1 + 1, \dots, M2$) successively updated and outputted from the second CIR estimating circuit 14.

[0096] Accordingly, in the receiver with a frequency offset correcting function according to Embodiment 2, the same effect as that in Embodiment 1 can be obtained, and further, when the equalizer 13b determines a data sequence of the transmitted signal, received signals after the second time and on are determined based on successively updated values of the CIR estimated values at the first position successively outputted from the second CIR estimating circuit 14b, so that even when the CIR estimated values varies with time, the variation can be followed, and data can be made decision at a low error rate.

[0097] It should be noted that description has been made with an ordinary equalizer 13b as a determining means in Embodiment 2, but a soft-decision equalizer 13a1 for executing soft-decision as shown in Fig. 3 is combined with a hard-decision circuit 13a2 for executing hard decision of a soft-decision value, and the soft-decision equalizer 13a1 may also compute soft-decision values based on the CIR estimated values $g_{i, n}$ successively updated and outputted from the second CIR estimating circuit 14, and similarly to the case of Embodiment 1, design of each components can also be change.

(3) Embodiment 3

[0098] Next description is made for a receiver with a frequency offset correcting function according to Embodiment 3 of the present invention.

[0099] Fig. 12 shows configuration of the receiver with a frequency offset correcting function according to Embodiment 3. It should be noted that, in the figure, the same reference numerals are assigned to the components corresponding to those in Embodiment 1 shown in Fig. 1.

[0100] In the figure, Embodiment 3 is characterized in that a local oscillator correcting circuit 19 is provided for correcting a frequency from a local oscillator 18 of the receiver with a frequency-offset estimated value outputted from the averaging circuit 16 in place of correcting frequency offset of the received signal in the frequency offset correcting circuit 11. For this reason, with Embodiment 3, the same effect as that of Embodiment 1 can be obtained.

(4) Embodiment 4

[0101] Next description is made for a receiver with a frequency offset correcting function according to Embodiment 4 of the present invention.

[0102] Fig. 13 is a block diagram showing an example of the receiver with a frequency offset correcting function according to Embodiment 2.

[0103] In the figure, designated at the reference numeral 211 to 21P (P: an arbitrary natural number) are P-units of frequency offset correcting circuits for receiving received signals $r_{n,1}$ to $r_{n,P}$ and correcting the received signals $r_{n,1}$ to $r_{n,P}$ based on frequency offset estimated values $\Delta \omega_m$ respectively; at 22 a first CIR estimating circuit for estimating CIR at the first position on a burst according to a training sequence in P-pieces of received signals $r'_{n,1}$ to $r'_{n,P}$ corrected by the P-units of frequency offset correcting circuit 21 respectively; at 23 an equalizer for estimating data sequence in the received signals according to the received signals $r'_{n,1}$ to $r'_{n,P}$ corrected by the frequency offset correcting circuits 211 to 21P as well as to each CIR estimated value at the first position estimated by the first CIR estimating circuit 22, and estimating, when a binary signal, for instance, 1 or -1 is transmitted, which value of 1 and -1 is the received signal r_n or the like; at 24 a second CIR estimating circuit for estimating each CIR estimated value at a second position apart from the first position on the burst according to the received signal $r'_{n,1}$ to $r'_{n,P}$ corrected by the frequency offset correcting circuits 211 to 21P, each CIR estimated value at the first position estimated by the first CIR estimating circuit 22, and to a result of decision in the equalizer 13; at 25 a phase deviation detecting circuit for computing a phase deviation according to the CIR estimated value at the first position estimated by the first CIR estimating circuit 22 as well as to the CIR estimated value at the second position estimated by the second CIR estimating circuit 24, and at 26 an averaging circuit for averaging the phase deviations detected by the phase deviation detecting circuit 25 and computing a frequency offset estimated value. It should be noted that the phase deviation detecting circuit 25 and averaging circuit 26 constitute a frequency-offset estimated value computing circuit 27.

[0104] Next description is made for operations of the receiver with a frequency offset correcting function according to Embodiment 4. It should be noted that a received signal comprises the burst B2 shown in Fig. 2 described in Embodiment 1, namely the training sequence B21 and the data sequence B22, and it is assumed that the burst B2 of which the

training sequence B21 has been known by the receiver is received.

[0105] At first, in Embodiment 4, the frequency offset correcting circuits 211 to 22P correct P-pieces of received signals $r_{n,p}$ respectively based on frequency-offset estimated values $\Delta \omega_{m-1}$ through the following equation.

$$r'_s = r_{n,p} \exp(-j \Delta \omega_{m-1} n) \quad (23)$$

[0106] Wherein, p indicates as follows: $p = 1, \dots, P$

[0107] Then, the first CIR estimating circuit 22 computes CIR estimated values $g_{0,n,p}, g_{1,n,p}, \dots, g_{L,n,p}$ with the LMS algorithm according to each known training sequence I_n as well as to each training sequence in the corrected P-pieces of received signals $r'_{n,p}$. It should be noted that the LMS algorithm is as follows.

$$g_{i,n,p} = g_{i,n-1,p} + \alpha \{r'_{n,p} - \sum_j g_{j,n-1,p} I_{n-j}\} I_{n-i}^* \quad (24)$$

[0108] Wherein, i, p and n indicate as follows: $i = 0, \dots, L$, $p = 1, \dots, P$, and $n = L + 1, \dots, M1$. Also, the sum Σ is obtained for $j = 0, \dots, L$. The reference sign α indicates a step size of the LMS algorithm, and initial values $g_{0,L,p}, g_{1,L,p}, \dots, g_{L,L,p}$ of the CIR estimated values are set to arbitrary values respectively. It should be noted that the reference sign M1 indicates a time corresponding to the final symbol of the training sequence.

[0109] Then, the equalizer 23 determines a data sequence according to the CIR estimated values $g_{0,M1,p}, g_{1,M1,p}, \dots, g_{L,M1,p}$ for P-pieces of received signal $r'_{n,p}$ corrected and outputted from the first CIR estimating circuit 22 as well as to the corrected P-pieces of received signal $r'_{n,p}$ and outputs a result of the decision as a decision value J_n .

[0110] Then, the second CIR estimating circuit 24 updates the CIR estimated values $g_{0,n,p}, g_{1,n,p}, \dots, g_{L,n,p}$ with the LMS algorithm according to the corrected received signals $r'_{n,p}$ as well as to the decision value J_n outputted from the equalizer 23 with the CIR estimated values $g_{0,M1,p}, g_{1,M1,p}, \dots, g_{L,M1,p}$ outputted from the first CIR estimating circuit 22 as initial values. It should be noted that updating is executed with the following equation:

$$g_{i,n,p} = g_{i,n-1,p} + \alpha \{r'_{n,p} - \sum_j g_{j,n-1,p} J_{n-j}\} J_{n-i}^* \quad (25)$$

wherein i, p and n indicate as follows: $i = 0, \dots, L$, $p = 1, \dots, P$, and $n = M1 + 1, \dots, M2$. Also, the sum Σ is obtained for $j = 0, \dots, L$. As for J_n in $n \leq M1$, a training sequence I_n is used in place of a decision value J_n .

[0111] Then, the phase deviation detecting circuit 25 detects a phase deviation according to the series described below. At first, any CIR estimated value of which the absolute value is maximum is selected as a tap coefficient among the CIR estimated values $g_{0,M1,p}, g_{1,M1,p}, \dots, g_{L,M1,p}$ outputted from the first CIR estimating circuit 22. Herein, it is assumed that a CIR estimated value of which the absolute value is maximum is a tap coefficient $g_{Max,M1}$. At the same time, the CIR estimated value $g_{Max,M2}$ corresponding to the tap coefficient $g_{Max,M1}$, namely i of which is the same between the coefficients, is selected among the CIR estimated values $g_{0,M2,p}, g_{1,M2,p}, \dots, g_{L,M2,p}$ outputted from the second estimating circuit 24, and a phase deviation Φ_m on a complex plane is computed with the following equation:

$$\Phi_m = g_{Max,M2} \cdot g_{Max,M1}^* \quad (26)$$

[0112] Herein, a^* indicates a complex conjugate of a complex number a.

[0113] Then, further, the phase deviation Φ_m on the complex plane is converted to a phase deviation ϕ_m on polar coordinates with the following equation:

$$\phi_m = \text{Im}[\Phi_m] / \text{Re}[\Phi_m] \quad (27)$$

[0114] Then, the averaging circuit 26 divides the phase deviation ϕ_m outputted from the phase deviation detecting circuit 25 by $(M2 - M1)$ to compute the phase deviation $\Delta \phi_m$ per symbol.

$$\Delta \phi_m = \phi_m / (M2 - M1) \quad (28)$$

[0115] Further, the averaging circuit 26 averages the phase deviation $\Delta \phi_m$ per symbol with a FIR filter expressed with the following equation, and outputs a result of the averaging as each frequency-offset estimated value $\Delta \omega_m$ to the frequency offset correcting circuits 211 to 21P.

$$\Delta \omega_m = \sum \Delta \phi_{m-j} / Q \quad (29)$$

wherein the sum Σ is obtained for $j = 1, \dots, Q$.

[0116] Then, each of the P-units of frequency offset correcting circuits 211 to 21P corrects each of received signals

$r_{n,p}$ based on the frequency-offset estimated value $\Delta \omega_m$ from the averaging circuit 16 through the equation (23) respectively.

[0117] As described above, with Embodiment 4 of the present invention, frequency offset is estimated without using known data such as tail bits other than the training sequence, and data can be determined while distortion of the frequency offset is compensated, so that, similarly to the case of Embodiment 1, the need for the known data such as tail bits other than the training sequence can be eliminated, transmission efficiency can be improved, even when frequency offset varies with time, the variation can be followed, time-varying frequency offset can be estimated with high precision, and further frequency offset can be corrected with a frequency-offset estimated value with less noise element.

[0118] Also, in Embodiment 4, a plurality of frequency offset correcting circuits 211 to 21P are provided, and each data sequence for a plurality of received signals $r_{n,p}$ is determined with the equalizer 23, so that diversity reception can be realized and a error rate of determined data can be reduced.

INDUSTRIAL APPLICABILITY

[0119] As described above, with the receiver with a frequency offset correcting function according to the present invention, CIR estimated values at first and second positions are obtained according to a known training sequence in a received signal, and a frequency-offset estimated value can be computed according to those phase deviations, so that frequency offset of the received signal can be corrected without using known data such as tail bits other than the training sequence, and data in the received signal can be determined.

[0120] As a result, the need for tail bits constituting a burst structure of the received signal is eliminated, so that transmission efficiency can be improved, and also phase deviations are not computed based on estimated values (replica) or the like only according to tail bits in a transmitted sequence but can be computed based on a channel impulse response estimated by sufficiently suppressing a noise element with an appropriate algorithm (LMS algorithm or the like), and for this reason large variation in a detected phase deviation due to noises can be eliminated, time-varying frequency offset can be compensated with high precision, and also data can be determined at a low error rate.

[0121] Also, determination of received signals at the second time and thereafter in a determining means can be made based on values, obtained by successively updating a CIR estimated value at the first position, outputted from the second estimating means, so that even when the CIR estimated value varies with time, determination can follow the variations, which allows data to be determined at a low error rate.

[0122] Also, as a frequency from a local oscillator of a receiver is directly controlled in place of correcting frequency offset of a received signal, so that the need for a frequency offset correcting circuit is eliminated, which allows configuration of a circuit for the receiver to be simple.

[0123] Also, as a plurality of received signals are received by a plurality of frequency offset correcting circuits respectively, diversity reception can be performed, which allows data to be determined at a low error rate.

[0124] In addition, decision including reliability is made with a soft-decision equalizer, which allows the reliability to be utilized in forward error correction and so on.

Claims

1. A receiver with a frequency offset correcting function comprising:

a frequency offset correcting means for receiving a received signal as well as a frequency-offset estimated value, and correcting phase rotation due to frequency offset of said received signal according to said frequency-offset estimated value;

a first channel impulse response estimating means for estimating channel impulse response at a first position of said corrected received signal according to a known training sequence included in the received signal corrected by said frequency offset correcting means;

a determining means for determining said received signal corrected by said frequency offset correcting means according to said channel impulse response estimated value at the first position thereof estimated by said first channel impulse response estimating means;

a second channel impulse response estimating means for estimating channel impulse response at a second position different from said first position of said corrected received signal according to said received signal corrected by said frequency offset correcting means, said channel impulse response estimated value at the first position thereof estimated by said first channel impulse response estimating means, and to the value determined by said determining means; and

a frequency-offset estimated value computing means for computing a frequency-offset estimated value of said received signal according to said channel impulse response estimated value at the first position thereof estimated by said first channel impulse response estimating means as well as to said channel impulse response

estimated value at the second position thereof estimated by said second channel impulse response estimating means, and outputting the computed value to said frequency offset correcting circuit.

2. A receiver with a frequency offset correcting function comprising:

a frequency offset correcting means for receiving a received signal as well as a frequency-offset estimated value and correcting phase rotation due to frequency offset of said received signal according to said frequency-offset estimated value;

a first channel impulse response estimating means for estimating channel impulse response at a first position of said corrected received signal according to a known training sequence included in the received signal corrected by said frequency offset correcting means;

a determining means for determining the received signal corrected by said frequency offset correcting means;

a second channel impulse response estimating means for estimating channel impulse response at a second position apart from said first position of said corrected received signal by updating said channel impulse response estimated value at the first position according to the received signal corrected by said frequency offset correcting means, said channel impulse response estimated value at the first position thereof estimated by said first channel impulse response estimating means, and to the value determined by said determining means; and

a frequency-offset estimated value computing means for computing a frequency-offset estimated value of said received signal according to said channel impulse response estimated value at the first position thereof estimated by said first channel impulse response estimating means as well as to said channel impulse response estimated value at the second position thereof estimated by said second channel impulse response estimating means, and outputting the computed value to said frequency offset correcting circuit; wherein

said determining means determines the received signal corrected by said frequency offset correcting means, at first, according to said channel impulse response estimated value at the first position thereof estimated by said first channel impulse response estimating means, and determines the received signal corrected by said frequency offset correcting means, after the second time and on, according to a value updated from said channel impulse response estimated value at the first position thereof by said second channel impulse response estimating means.

3. A receiver with a frequency offset correcting function comprising:

a first channel impulse response estimating means for estimating channel impulse response at a first position of said received signal according to a known training sequence included in the received signal;

a determining means for determining the received signal corrected by said frequency offset correcting means according to said channel impulse response estimated value at the first position thereof estimated by said first channel impulse response estimating means;

a second channel impulse response estimating means for estimating channel impulse response at a second position apart from said first position of said received signal according to the received signal corrected by said frequency offset correcting means, said channel impulse response estimated value at the first position thereof estimated by said first channel impulse response estimating means, and to the value determined by said determining means;

a frequency-offset estimated value computing means for computing a frequency-offset estimated value of said received signal according to said channel impulse response estimated value at the first position thereof estimated by said first channel impulse response estimating means as well as to said channel impulse response estimated value at the second position thereof estimated by said second channel impulse response estimating means; and

a local oscillator correcting means for correcting a frequency from a local oscillator according to the frequency-offset estimated value computed by said frequency-offset estimated value computing means.

4. A receiver with a frequency offset correcting function comprising:

a frequency offset correcting means for receiving a plurality of received signals as well as frequency-offset estimated value, and correcting each phase rotation due to frequency offset for said plurality of received signals according to said frequency-offset estimated value respectively;

a first channel impulse response estimating means for estimating each channel impulse response at a first position of said plurality of corrected received signals according to each known training sequence included in said plurality of received signals corrected by said frequency offset correcting means;

a determining means for determining said plurality of received signals corrected by said frequency offset correcting means according to said channel impulse response estimated values each at the first position thereof estimated by said first channel impulse response estimating means;

a second channel impulse response estimating means for estimating each channel impulse response at a second position apart from the first position of the plurality of corrected received signals according to said plurality of received signals corrected by said frequency offset correcting means, each channel impulse response estimated value at the first position of said plurality of corrected received signals estimated by said first channel impulse response estimating means, and to the value of said plurality of received signals determined by said determining means; and

a frequency-offset estimated value computing means for computing frequency-offset estimated value of said plurality of received signals according to each channel impulse response estimated value at the first position thereof estimated by said first channel impulse response estimating means as well as to each channel impulse response estimated value at the second position thereof estimated by said second channel impulse response estimating means, and outputting the computed value to said frequency offset correcting circuit.

5. A receiver with a frequency offset correcting function according to claim 1; wherein the frequency-offset estimated value computing means comprises:

a phase deviation detecting means for detecting a phase deviation between said first position and said second position according to the channel impulse response estimated value at the first position estimated by the first channel impulse response estimating means as well as to the channel impulse response estimated value at the second position estimated by the second channel impulse response estimating means; and

an averaging means for averaging phase deviations obtained by computing a phase deviation per symbol according to the phase deviation between said first position and said second position detected by said phase deviation detecting means to compute a frequency-offset estimated value, and outputting the computed value to the frequency offset correcting circuit.

6. A receiver with a frequency offset correcting function according to claim 5; wherein the phase deviation detecting means:

selects a value of which the absolute value is maximum among the channel impulse response estimated values at the first position estimated by the first channel impulse response estimating means, and also selects a value corresponding to said channel impulse response estimated value at the first position of which the absolute value is maximum among the channel impulse response estimated values at the second position estimated by the second channel impulse response estimating means; and
detects a phase deviation of the received signal according to the product of complex conjugate of said channel impulse response estimated value at the first position of which the absolute value is maximum and said channel impulse response estimated value at the second position corresponding to the channel impulse response estimated value at the first position of which the absolute value is maximum.

7. A receiver with a frequency offset correcting function according to claim 5; wherein the phase deviation detecting means:

computes each product of the complex conjugate of the channel impulse response estimated value at the first position estimated by the first channel impulse response estimating means and the channel impulse response estimated value at the second position estimated by the second channel impulse response estimating means, and detects a phase deviation of the received signal according to the sum of the products each of which the absolute value is more than a threshold value among the computed products.

8. A receiver with a frequency offset correcting function according to claim 5; wherein the phase deviation detecting means:

computes each product of the complex conjugate of the channel impulse response estimated value at the first position estimated by the first channel impulse response estimating means and the channel impulse response estimated value at the second position estimated by the second channel impulse response estimating means, selects each product of which the absolute value is more than a threshold value among the computed products, multiplies each of the absolute values to the selected products, and detects the phase deviation of the received signals according to the sum of the multiplied values.

9. A receiver with a frequency offset correcting function according to claim 5; wherein the phase deviation detecting means:

5 further quantizes the phase deviation of the detected received signal, and outputs a result of the quantization as a phase deviation.

10. A receiver with a frequency offset correcting function according to claim 5; wherein the determining means comprises:

10 a soft-decision equalizer for executing soft-decision of a data sequence in the corrected received signal according to said received signal corrected by the frequency offset correcting means as well as to the channel impulse response estimated value at the first position estimated by the first channel impulse response estimating means; and

15 a hard-decision circuit for executing hard decision of the soft-decision value estimated by said soft-decision equalizer and outputting a result of the decision as a decision value of a data sequence in the received signal.

20

25

30

35

40

45

50

55

FIG.1

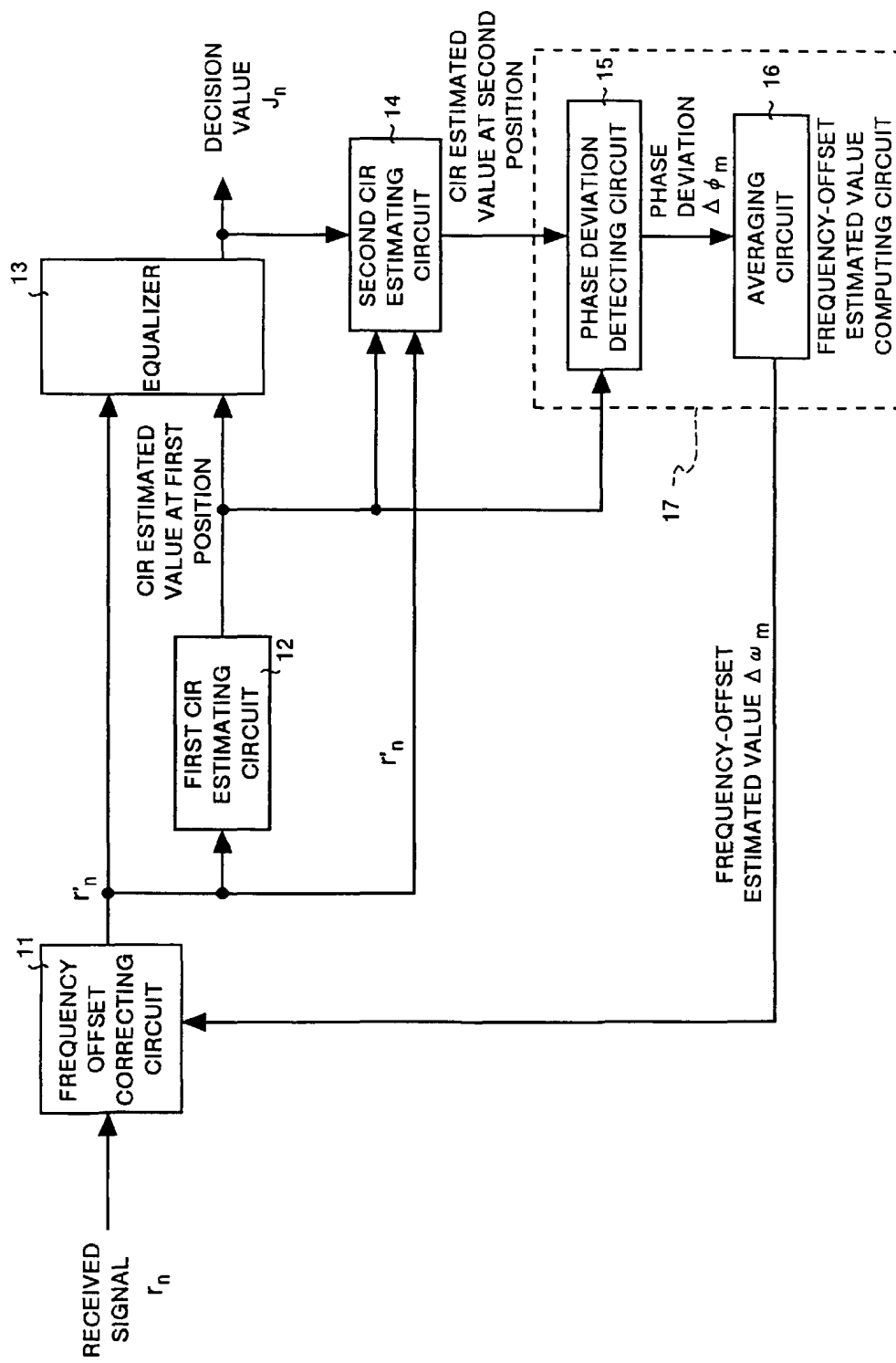


FIG.2

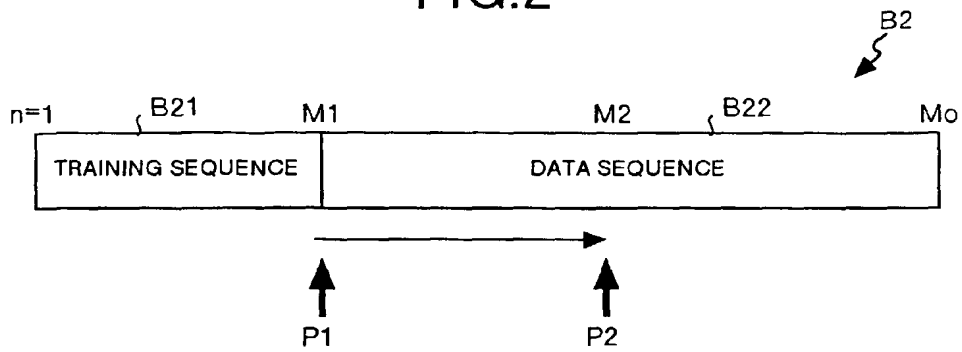


FIG.3

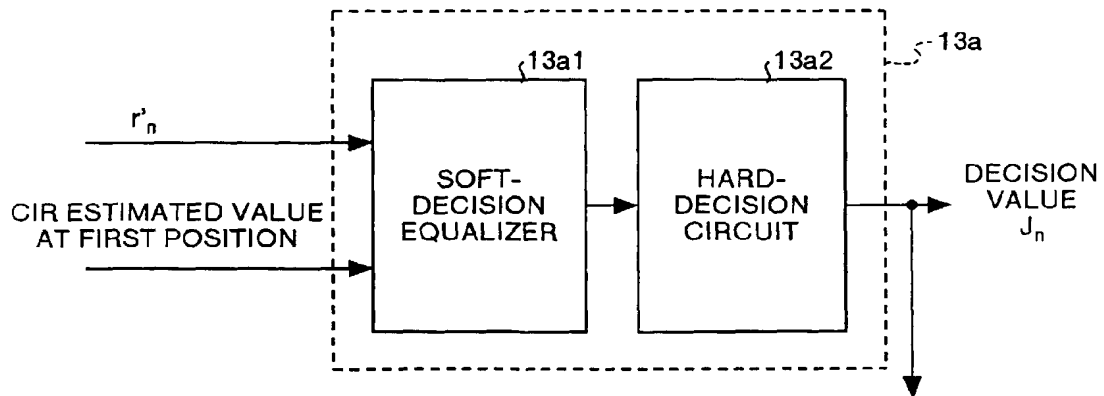


FIG.4

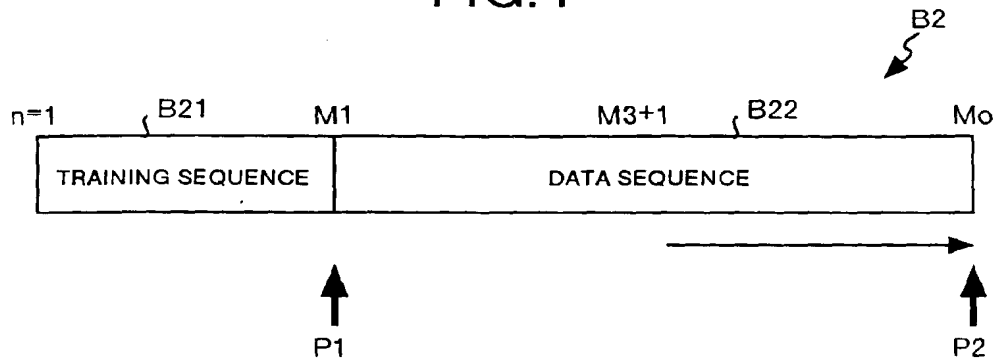


FIG.5

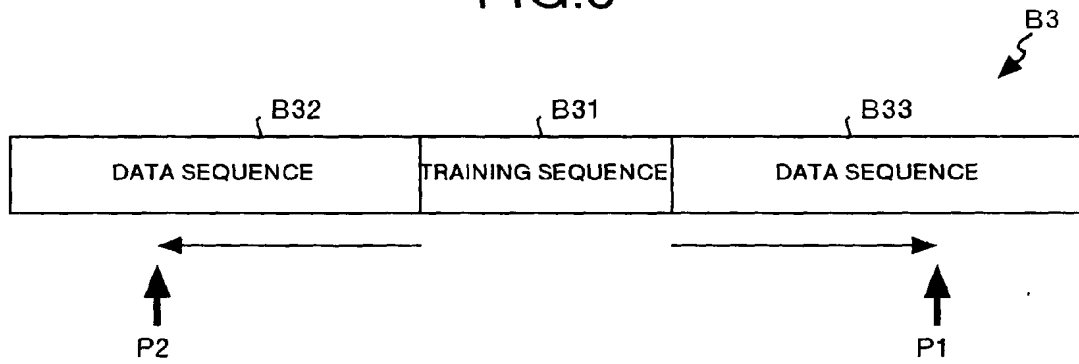


FIG.6

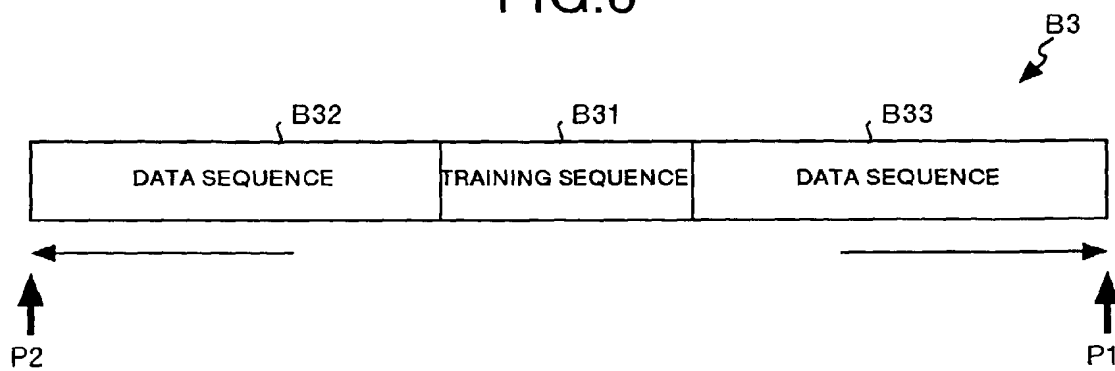


FIG.7

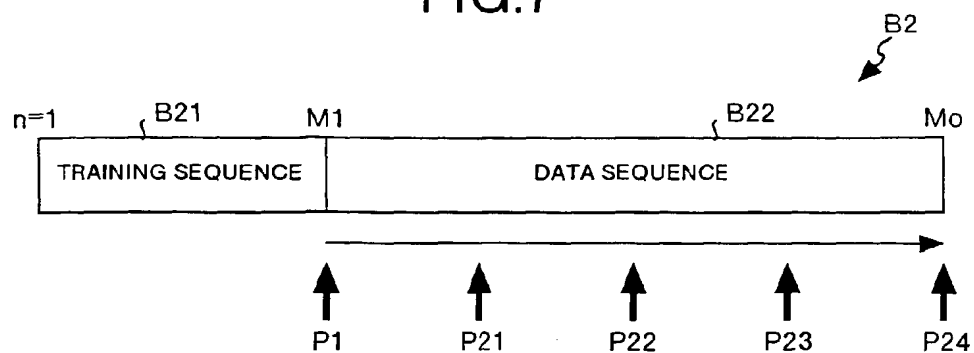


FIG.8

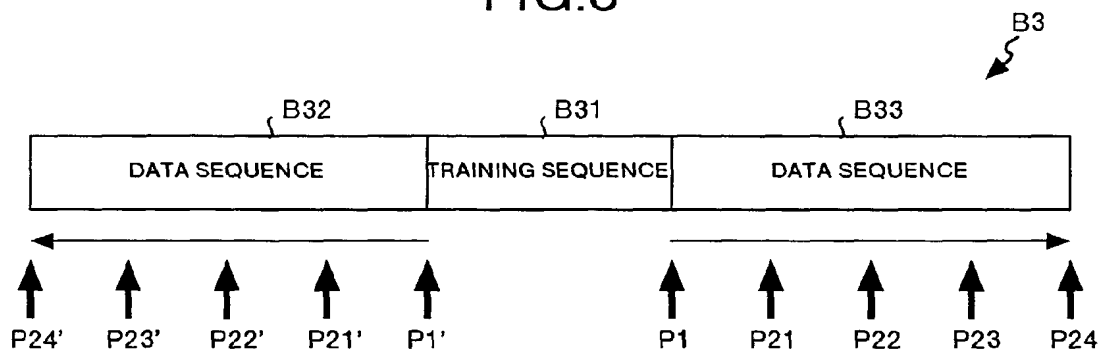


FIG.9

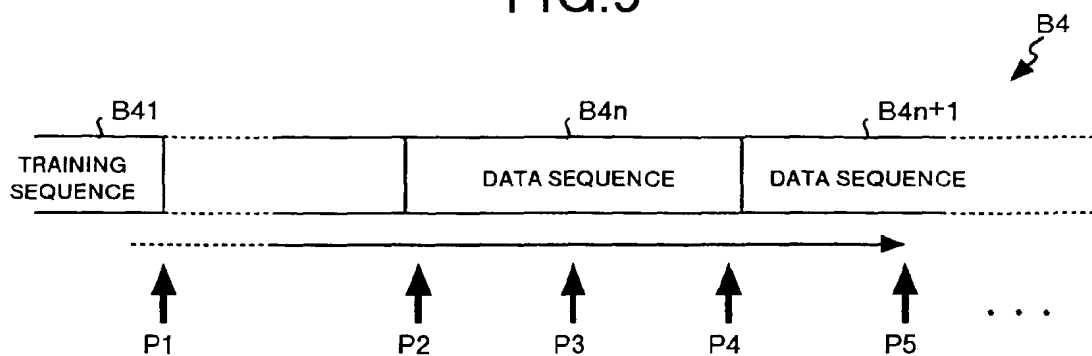


FIG.10

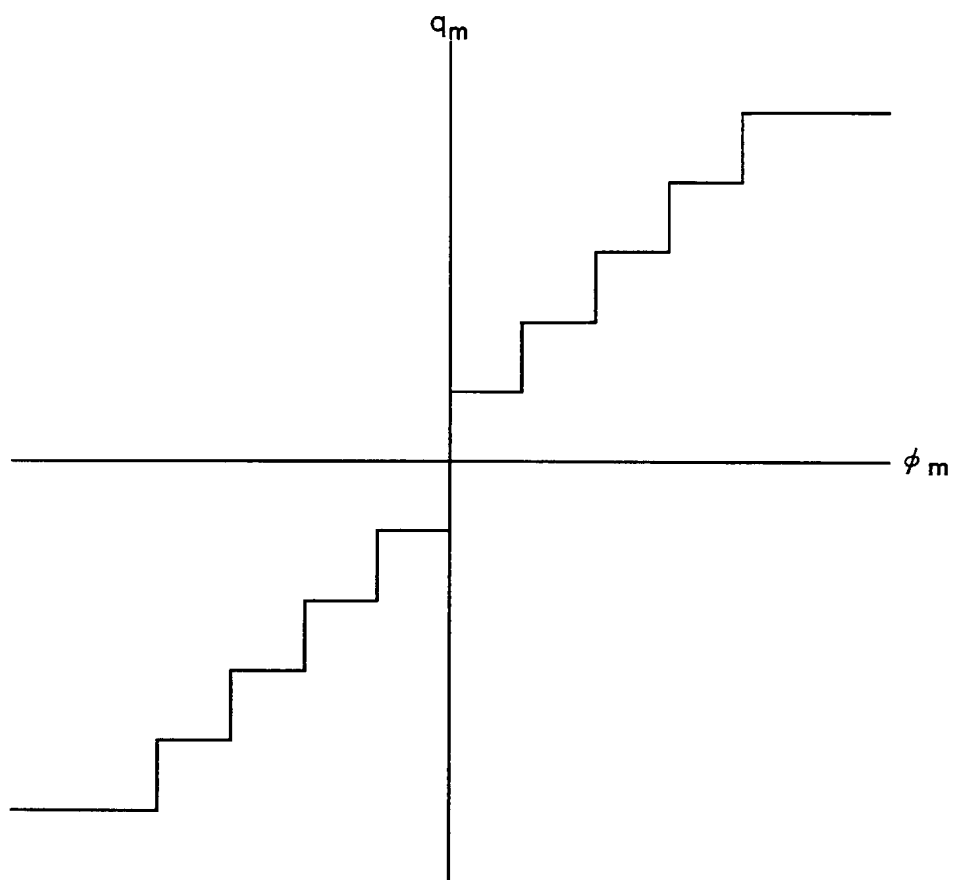


FIG.11

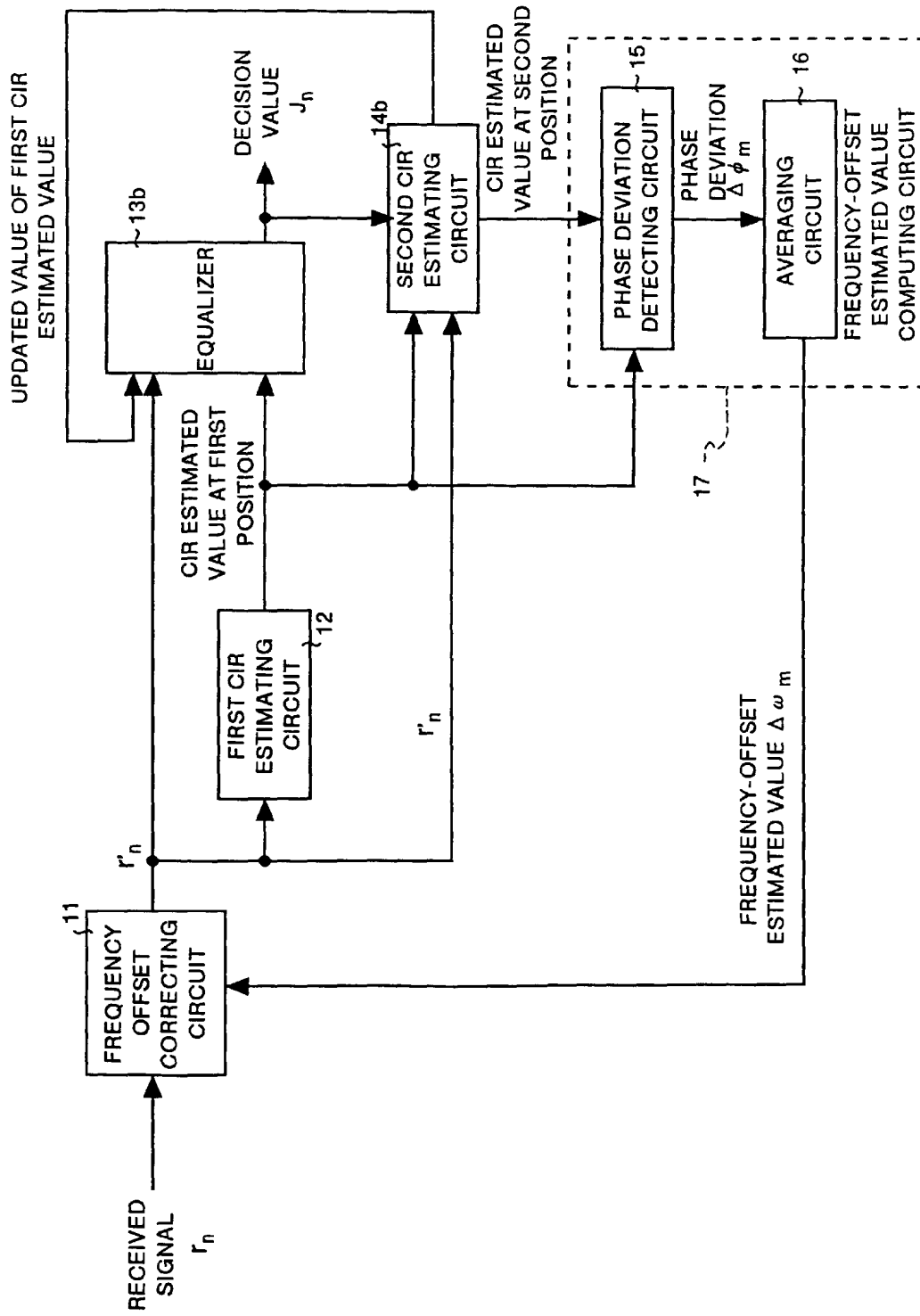


FIG.12

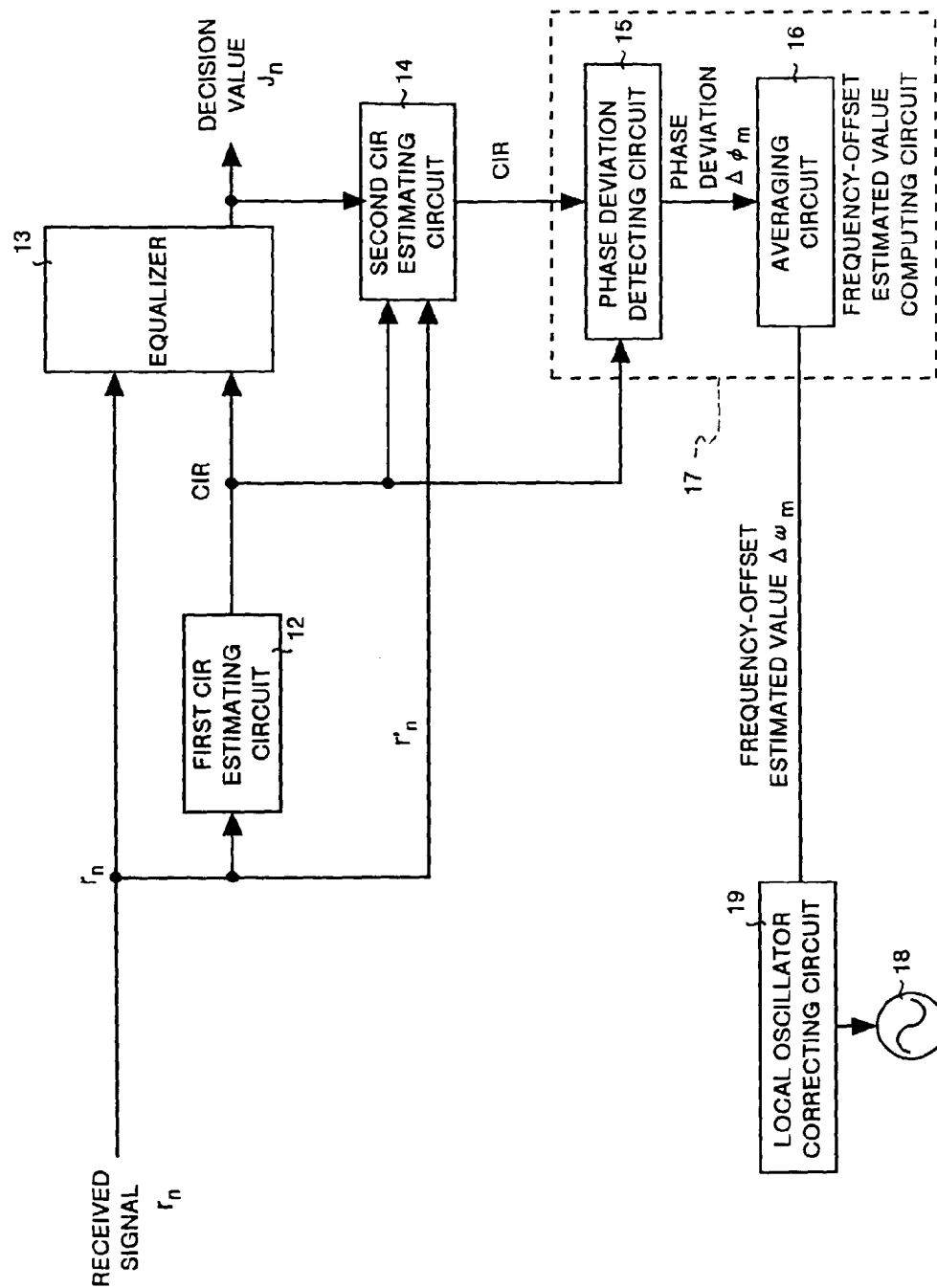


FIG.13

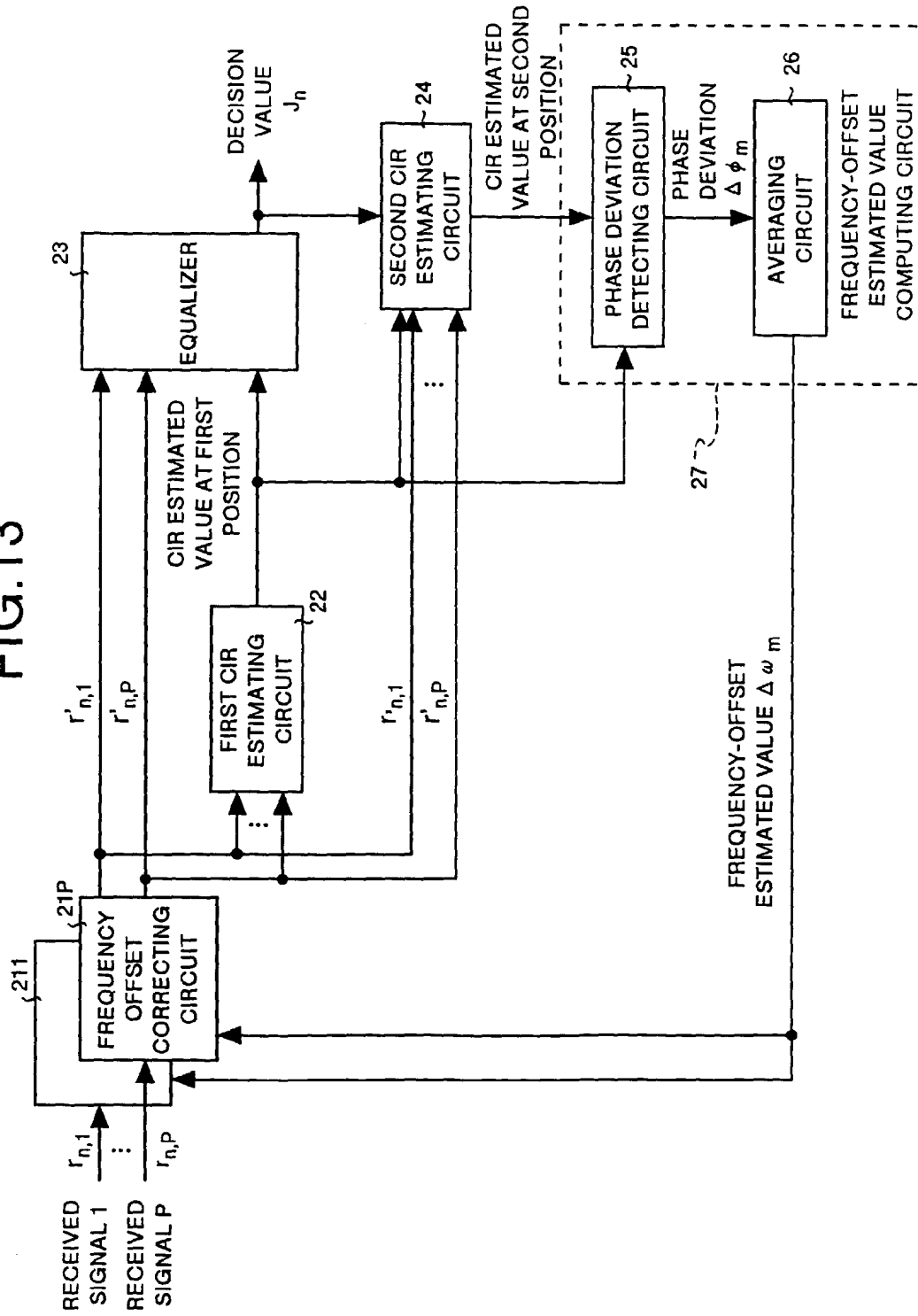


FIG.14

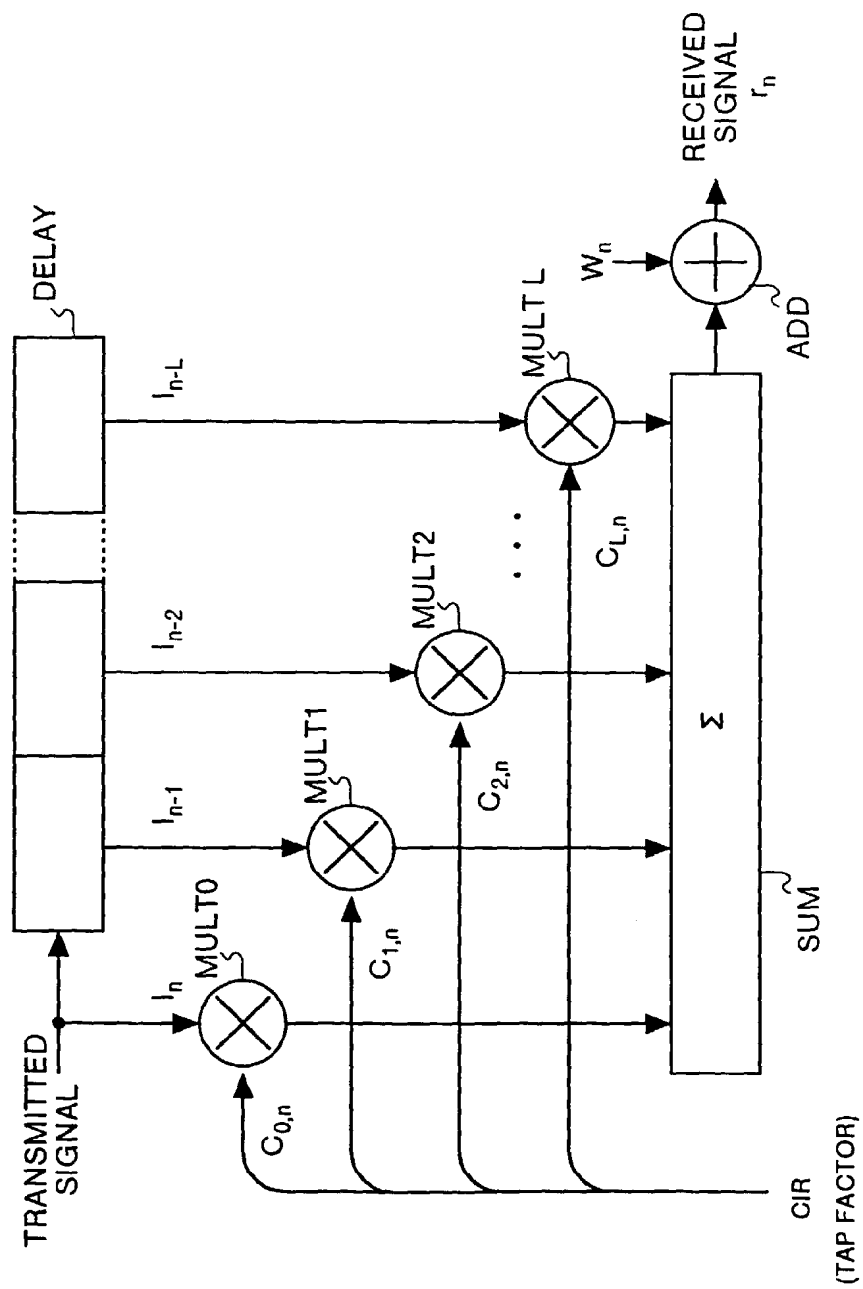


FIG.15

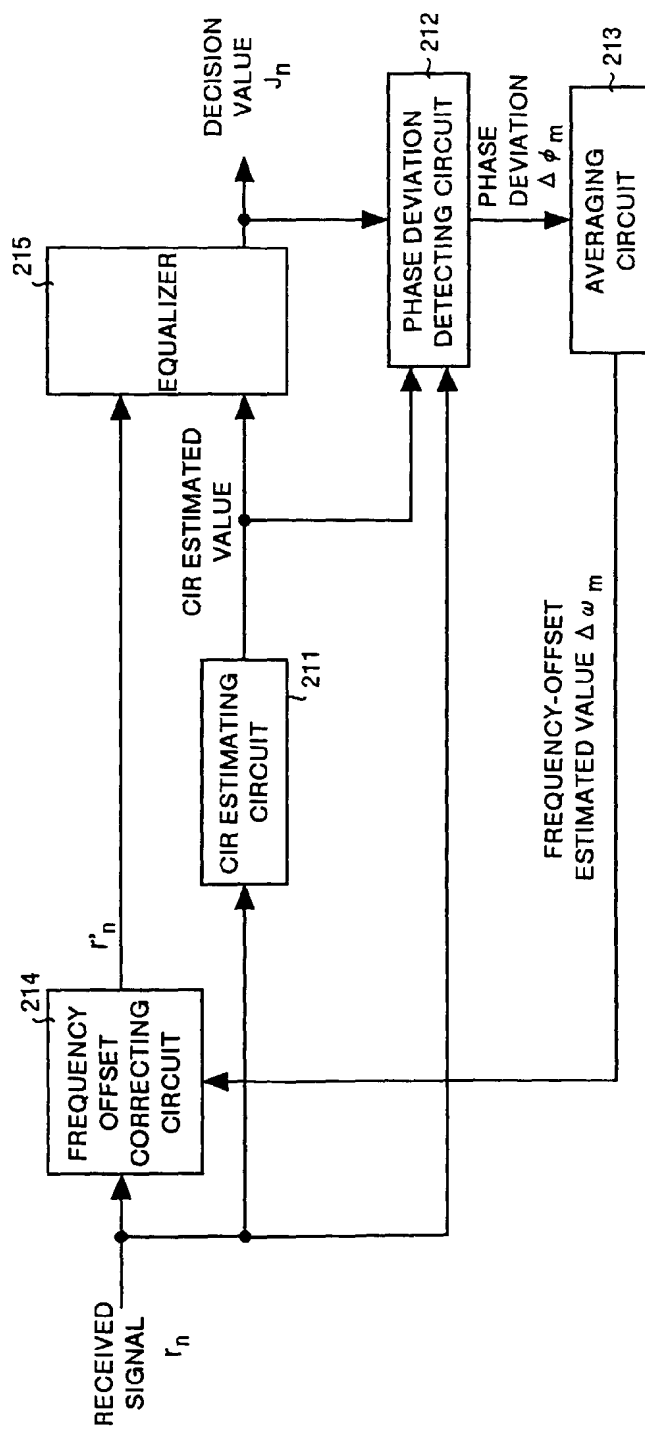
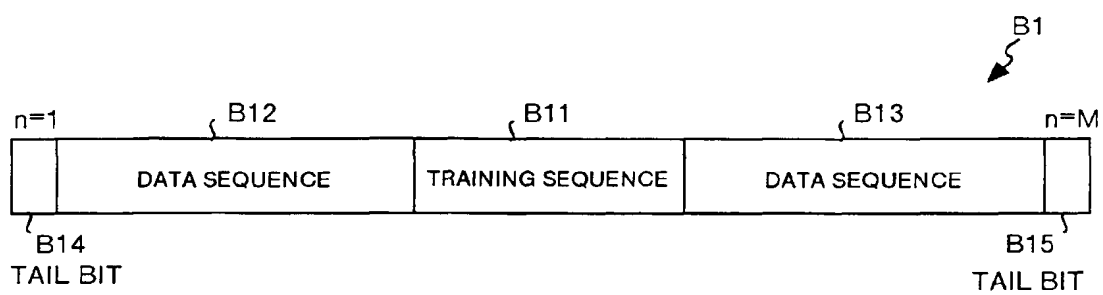


FIG.16



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP97/00653

A. CLASSIFICATION OF SUBJECT MATTER Int. Cl ⁶ H04B3/10 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) Int. Cl ⁶ H04B3/10, H04L27/14, 27/22, H04B7/005 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Jitsuyo Shinan Koho 1926 - 1997 Kokai Jitsuyo Shinan Koho 1971 - 1997 Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 6-508244, A (Motorola, Inc.), September 14, 1994 (14. 09. 94), Page 5, upper left column, line 14 to page 7, upper right column, line 7; Fig. 3 & AU, 9218909, A & US, 5245611, A & EP, 587641, A1	1 - 10
A	JP, 8-223096, A (Kokusai Electric Co., Ltd.), August 30, 1996 (30. 08. 96), Page 3, left column, line 16 to page 4, right column, line 38 (Family: none)	1 - 10
A	JP, 4-502692, A (Motorola, Inc.), May 14, 1992 (14. 05. 92), Page 3, lower left column, line 10 to page 5, upper left column, line 6 & EP, 373405, A & CA, 2003580, A	1 - 10
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search May 26, 1997 (26. 05. 97)		Date of mailing of the international search report June 10, 1997 (10. 06. 97)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.		Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)